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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	09/511,737
				Filing Date	February 24, 2000
				First Named Inventor	YELLIN, Daniel
				Group Art Unit	2124
				Examiner Name	MAI, Tan V.
Sheet	1	of	2	Attorney Docket Number	P-5332-US

[illegible][illegible]

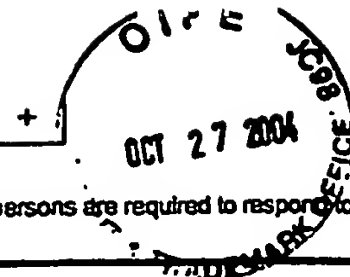
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Substitute for form 1449B/PTO		Complete if Known	
		Application Number	09/511,737
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Filing Date	February 24, 2000
		First Named Inventor	YELLIN, Daniel
		Group Art Unit	2124
		Examiner Name	MAJ, Tan V.
(use as many sheets as necessary)		Attorney Docket Number	P-5332-US
Sheet	2	of	2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (where appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
man ↓ ✓	B	UMING KO et al., "A Self-Timed Method to Minimize Spurious Transitions in Low Power CMOS Circuits", Low Power Electronics, 1994, Digest of Technical Papers, IEEE Symposium, San Diego CA, USA, 10 OCT 1994, pp. 82-83	<input type="checkbox"/>
	C	Vivek Tiwari, "Guarded evaluation: pushing power management to logic synthesis/design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 10, 10 OCT 1998, pp. 1051-1060	<input type="checkbox"/>
	D	Supplementary Search Report for EP 01 80 8088	<input type="checkbox"/>
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